CLAIMS

What is claimed is:

1. A method for reading a flash memory cell comprising:
accessing leakage current of a common bit line comprising said flash memory cell;
accessing read current of said flash memory cell;
eliminating said leakage current from said read current to determine a cell current; and
comparing said cell current to a verify cell current.

2. The method as described in Claim 1 wherein said verify cell is a read verify cell.

3. The method as described in Claim 1 wherein said verify cell is an erase verify cell.

4. The method as described in Claim 1 wherein said flash memory cell is disposed in an array of flash memory cells, said cells arranged with at least one common word line and one common bit line

5. The method as described in Claim 1 wherein said accessing leakage current comprises configuring said flash memory cell for a read operation with a control gate voltage at approximately zero volts.

6. The method as described in Claim 5 wherein said control gate is an element of said common word line.

7. The method as described in Claim 1 wherein said eliminating said leakage current from said read current comprises subtracting a voltage corresponding to said read current from a voltage corresponding to said leakage current.

8. The method as described in Claim 7 wherein said voltage corresponding to said leakage current is stored on a capacitive element.

9. The method as described in Claim 1 wherein said flash memory cell comprises a floating gate as a storage element.

10. The method as described in Claim 1 wherein said flash memory cell comprises a nitride layer as a storage element.

11. A method of erasing a sector of flash memory comprising:
applying an erase pulse to said sector of flash memory;
performing a method for verifying erasure of each flash memory cell in said sector of flash memory, said method comprising:
accessing leakage current of a common bit line comprising said flash memory cell;
accessing read current of said flash memory cell;

eliminating said leakage current from said read current to determine a cell current;

comparing said cell current to an erase verify cell current; and

repeating said applying an erase pulse if said cell current is greater than said erase verify cell current.

12. The method as described in Claim 11 wherein said accessing leakage current comprises configuring said flash memory cell for a read operation with a control gate voltage at approximately zero volts.

13. The method as described in Claim 11 wherein said eliminating said leakage current from said read current comprises subtracting a voltage corresponding to said read current from a voltage corresponding to said leakage current.

14. The method as described in Claim 13 wherein said voltage corresponding to said leakage current is stored on a capacitive element.

15. The method as described in Claim 11 wherein said flash memory cell comprises a floating gate as a storage element.

16. The method as described in Claim 11 wherein said flash memory cell comprises a nitride layer as a storage element.

17. An integrated circuit device comprising:

an array of flash memory cells, said cells arranged with at least one common word line and at least one common bit line;

first circuitry for accessing a leakage current of said common bit line, coupled to said common bit line;

second circuitry for accessing a read current of a flash memory cell of said common bit line, coupled to said common bit line; and

third circuitry for eliminating said leakage current from said read current to determine a cell current, coupled to said first and second circuitry.

18. The integrated circuit of Claim 17 wherein said first circuitry applies approximately zero volts to a control gate of said flash memory cell.

19. The integrated circuit of Claim 18 wherein said control gate is a portion of said common word line.

20. The integrated circuit of Claim 17 comprising a floating gate as a storage element.

21. The integrated circuit of Claim 17 comprising a nitride layer as a storage element.